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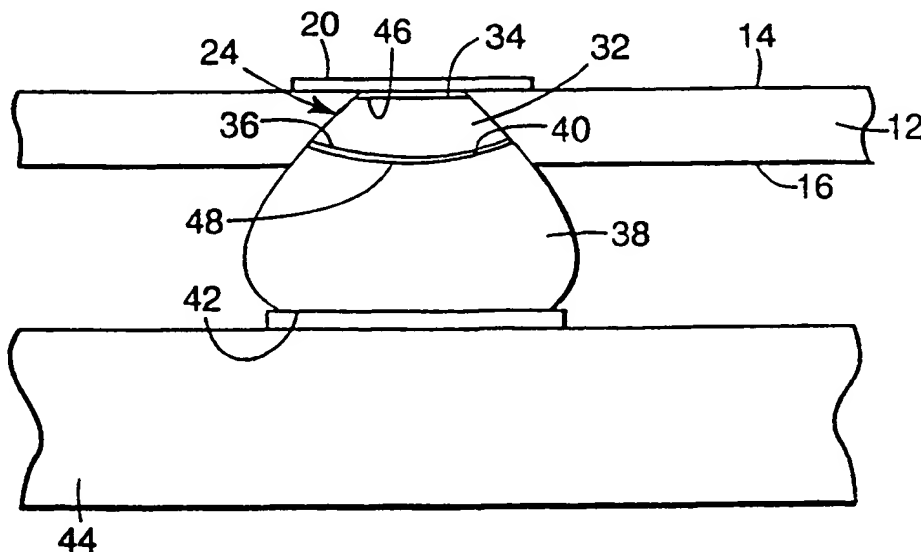
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(54) Title: THROUGH HOLE BUMP CONTACT



(57) Abstract

A circuit includes a substrate having a dielectric layer with a first surface and a second surface. A conductive layer is formed on the first surface. A beveled via is formed in a dielectric layer of the substrate. The via has a first opening of a first width in the first surface, and a second opening of a second width in the second surface, the second width being greater than the first width. A conductive plug is connected to the conductive layer. The plug is formed in the via and extends from adjacent the first opening toward the second opening, and terminates adjacent the second opening at a plug interface surface. A conductive solder ball is connected to the plug interface surface and extends to protrude from the second surface.

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THROUGH HOLE BUMP CONTACT

Background

The disclosures herein relate generally to solder ball electronic interconnections and more particularly to a via plug adapter for strengthening a solder ball connection in a beveled via.

Vertical interconnects between circuit layers is well known. U.S. Patent 3,541,222 discloses a connector screen for interconnecting aligned electrodes of adjacent circuit boards or modules. The connector screen comprises a matrix of spaced conductive connector elements embedded in a supporting non-conducting material with the conductive connector elements protruding from both sides thereof. The size and spacing of the connector elements are chosen so that the connector screen can be disposed between the circuit boards or modules to provide the required interconnections between the electrodes without requiring alignment of the connector screen with respect to the boards or modules. A preferred method of making the connector screen involves forming a conductive mold having a grid pattern of ridges in a non-conductive base. Conductive material is then cast between the ridges of the mold, following which selected portions of the mold are removed to form a web of non-conductive material supporting a matrix of spaced conducting elements protruding from both sides of the web.

U.S. Patent 4,830,264 describes a method of forming solder terminals for a pinless module, preferably for a pinless metallized ceramic module. The method is comprised of the following steps: forming a substrate having a pattern of conductors formed onto its top surface and preformed via-holes extending from the top to bottom surface; applying a droplet of flux at at least one of the preformed via-hole openings of the bottom surface of the substrate to fill the via-holes with flux by capillarity and form a glob of flux at the bottom openings; applying a solder preform, i.e. solder balls on each glob of flux to which it will adhere, the volume of the preform being substantially equal to the inner volume of the via-hole plus the volume of the bump to be formed; heating to cause solder reflow of the solder preform to fill the via-hole and the inner volume of the eyelet with solder; and, cooling below the melting point of the solder so that the molten solder solidifies to form solder terminals at the via-hole locations while forming solder columns in the via-holes. The resultant pinless

metallized ceramic module has connections between the I/O's of the module interfacing with the next level of packaging (i.e., printed circuit boards), that consist of integral solder terminals. Each integral solder terminal comprises a column in the vias of the metallized ceramic substrate, a mound of solder at the top surface of the substrate and spherical solder bumps on the bottom level for making interconnections with the next level of packaging.

In U.S. Patent 5,401,913, a multi-layer circuit board includes electrical interconnections between adjacent circuit board layers of the multi-layer board. A via hole is provided through a circuit board layer. The via hole is filled with a via metal. The via metal is plated with a low melting point metal. An adhesive film is deposited over the circuit board layer. Adjacent layers of the multi-layer circuit board are stacked and aligned together. The layers are laminated under heat and pressure. The low melting point metal provides an electrical interconnection between adjacent layers.

U.S. Patent 5,491,303 discloses an interposer for connecting two or more printed circuit boards comprising a circuit-carrying substrate with two or more solder pads on each of two sides. Each of the solder pads are connected to an electrically conductive via in the substrate, providing electrical interconnection from one side to the other side. Each solder pad has a solder bump on it. A circuit assembly is made by soldering the solder bumps on one side of the interposer to corresponding solder pads on a printed circuit board. The solder bumps on the other side of the interposer are likewise soldered to the corresponding solder pads of a second printed circuit board.

U.S. Patent 5,600,884 describes an electrical connecting member, one surface of which is connected to a connecting section of a first electrical circuit member and another surface of which is connected to a connecting section of a second electrical circuit member. The electrical connecting member includes a holding member formed of an electrically insulative member. The holding member has a plurality of recess holes. The connecting member also includes a plurality of electrically conductive members provided in the electrically insulative member, insulated from each other. One end of the electrically conductive members is exposed on one surface of the holding member to be connected to the connecting section of the first electrical circuit member. Another end of the electrically conductive members is exposed on

another surface of the holding member to be connected to the connecting section of the second electrical circuit member.

U.S. Patent 5,726,497 discloses a method of manufacture of a semiconductor device on a silicon semiconductor substrate which comprises formation of a first stress layer on the semiconductor substrate, formation of an interconnect layer over
5 the first stress layer, formation of a second stress layer on the interconnect layer, formation of an inter-metal dielectric (IMD) layer over the second stress layer, patterning and etching a via opening through the inter-metal dielectric layer and the second stress layer, exposing a contact area on the surface of the metal interconnect
10 layer, and heating the device at a temperature sufficient to squeeze the metal interconnect layer up into the via.

U.S. Patent 5,757,078 discloses a semiconductor device including a semiconductor chip having electrode pads, a package composed of a plurality of insulating films and adhered to the semiconductor chip by an adhesive agent. The
15 package includes wiring patterns interposed between the plurality of insulating films. The wiring patterns are selectively connected to the electrode pads at one end, and to the plurality of electrically conductive protrusions at the other end, by means of via-holes. The semiconductor device further includes a plurality of electrically
20 conductive protrusions extending from the outermost wiring patterns by way of the via-holes provided in the outermost insulating film.

Japanese Application JP 10-41356 discloses a tape carrier that is used as the bonding medium when semiconductor elements are bonded to the outer part of a substrate board for a BGA application. An insulating film includes vias having straight or non-tapered walls. A conductive land is formed in the vias and solder balls
25 have one side engaged with the lands inside of the vias. The remainder of each solder ball protrudes from the insulating film.

The use of flexible circuitry in IC packaging has been a growing trend for many years where the use of via connections through the flexible circuit dielectric have been employed in Tape Ball Grid Array (TBGA) IC packaging applications and
30 recently, into Chip Scale Packaging (CSP) applications. In Ball Grid Array (BGA) applications, the via interconnection traditionally uses a solder ball reflowed first to connect to the flexible circuitry through the via, then second, reflowed onto the printed circuit board with conventional surface mount assembly practices.

This solder ball connection must make a reliable electronic interconnect from the flexible circuitry to the printed circuit board. This reliability is often directly related to the area of the solder connection to the flexible circuitry, as a common failure mode of this interconnection is the solder ball shearing through the solder material at the point of the minimum cross sectional area. Therefore, larger vias are desirable to increase the area in which shear stress is distributed to meet minimum solder ball interconnection reliability requirements.

Conversely, the demand for smaller electronic packages and higher input/output (I/O's) requires increased routing density, including smaller via sizes to allow electronic traces to route between solder ball via areas. Smaller vias require smaller via capture pads, thus, allowing more space to route electronic traces between printed circuit board interconnection vias.

Traditionally, vias in the dielectric are made by punching, leaving a via through the dielectric with straight walls. Other methods include chemically dissolving the dielectric and laser drilling to expose the metal conductor of the flexible circuitry. Direct solder ball attachment to any of these via methods controls the solder ball interconnection reliability by means of the via size, such that, vias typically have to be larger than 0.200 mm in diameter to meet minimum reliability requirements for the electronic package.

Therefore, what is needed is an apparatus and a method for providing a strong and reliable solder ball connection to flexible circuitry with small diameter vias and via capture pads so as to permit more space in which to route more electronic traces.

Summary

One embodiment, accordingly, provides a strength enhanced solder ball connection to flexible circuitry with small diameter vias which improves the routability of the flexible circuit to address higher I/O and finer pitch flex based BGA packaging applications. To this end, a circuit comprises a substrate including a dielectric layer having a first surface and a second surface. A conductive layer is on the first surface. A beveled via is formed in the dielectric layer and has a first opening of a first width in the first surface, and a second opening of a second width in the second surface, greater than the first width. A conductive plug is formed in the via, connected to the conductive layer, and extends from adjacent the first opening toward

the second opening. The plug terminates adjacent the second opening at a plug interface surface. A conductive solder ball is connected to the plug interface surface and extends to protrude from the second surface.

A principal advantage of this embodiment is that the via adapter plug enables
5 a reliable solder ball connection to flexible circuitry with small (less than 0.200 mm diameter) vias. Using the via plug adapter concept, solder ball interconnection reliability does not have to be compromised to accommodate the routing requirements of high I/O, fine pitch flex based IC packaging applications. Using common design rules for flexible circuitry, a smaller via allows for a smaller via capture pad, thus,
10 more space between via capture pads in which to route electronic traces.

Brief Description of the Drawings

Fig. 1 is a side view illustrating an embodiment of a substrate interconnected to a circuit board by a plurality of solder balls.

Fig. 1A is a top view illustrating a circular via opening.

15 Fig. 1B is a top view illustrating an oblong via opening.

Fig. 2 is a side view illustrating an embodiment of a plug in a tapered via.

Fig. 3 is another side view illustrating an embodiment of a plug in a tapered via.

20 Fig. 4 is another side view illustrating an embodiment of a plug in a tapered via.

Fig. 5 is a side view illustrating an embodiment of a substrate interconnected to a circuit board by a solder ball.

Fig. 6 is a side view illustrating an embodiment of a two-layered substrate interconnected to a circuit board by solder ball.

25 Fig. 7 is a side view illustrating an embodiment of a chip scale package including an IC chip connected to a substrate.

Fig. 8 is a view of the substrate taken along line 8-8 of Fig. 7.

Detailed Description

According to one embodiment, Fig. 1, a flexible circuit 10 comprises a
30 substrate 12 formed of a flexible dielectric material. The substrate 12 is of a polymer or other suitable material having a thickness T1 of from 12 micrometers to 25 micrometers. The polymer may be a polyimide, a polyester, or other known polymers

for electronic applications. Substrate 12 also includes a first surface 14 and a second opposite surface 16. A conductive layer 18, of copper, gold plated copper, gold or other suitable material, is formed on first surface 14 and includes a plurality of conductive capture pads 20 and a plurality of conductive traces 22 routed between the capture pads 20.

A plurality of beveled vias 24 are formed in substrate 12. Each via 24 has a first opening 26 of a first width W1, in first surface 14, and a second opening 28 of a second width W2, in the second surface 16. Second width W2 is greater than first width W1. Beveled via 24 includes a sidewall 30 which is sloped away from first surface 14 at an angle α of from 20 degrees to 80 degrees, and preferably at an angle of from 20 degrees to 45 degrees. First opening 26 is circular, Fig. 1A, or oblong, Fig. 1B or may be of another suitable shape and first width W1 is from 0.05 mm to 0.5 mm.

A conductive plug 32, Figs 1 and 2 is formed in beveled via 24, and extends from a first plug interface surface 34, adjacent first opening 26, toward the second opening 28. Plug 32 terminates adjacent the second opening 28 at a second plug interface surface 36. The first plug interface surface 34 is connected to conductive capture pad 20. The second plug interface surface 36 is of a dome shape. Second plug interface surface 36 may be formed to terminate between first surface 14 and second surface 16, may be formed such that a portion of the dome extends outwardly from the second surface 16, Fig. 3, or may be formed such that the entire dome-like surface extends outwardly from the second surface 16, Fig. 4. Thus, a range of plug thickness or height T2 extending from first plug interface surface 34 to second plug interface surface 36 may vary, but is at least 5 microns, Fig. 2.

A conductive solder ball 38, Fig. 5, is connected to second plug interface surface 36 at a first solder ball surface 40, and protrudes from second substrate surface 16. Solder ball 38 terminates at a second solder ball surface 42 which may engage a printed circuit board 44. Plug 32 and solder ball 38 may be formed of various suitable materials. For example, plug 32 may be formed of a high temperature tin-lead solder engaged with solder ball 38 formed of a eutectic tin-lead solder. Also, plug 32 may be formed of copper engaged with solder ball 38 formed of a tin-lead solder. Other combinations may be used which meet the conductivity requirement and meet the condition that they provide the plug material of a stronger

shear strength than the solder ball material. As a further example, plug 32 may be formed of nickel engaged with solder ball 38 formed of a tin-lead solder. In addition, for improved bonding, an interface coating 46 may be provided between capture pads 20 and first plug interface surface 34. Coating 46 may be formed of a suitable material selected from gold, palladium and nickel-gold. Furthermore, bonding between plug 32 and solder ball 38 may be improved by another interface coating 48 therebetween. Coating 48 may be formed of a suitable material also selected from gold, palladium and nickel-gold.

Beveled vias 24, Fig. 1, are spaced apart in a side-by-side configuration.

Capture pads 20 are formed at each first opening 26. Therefore, capture pads 20 are also spaced apart in a side-by-side configuration. Spacing between vias 24 is of a center-to-center distance D of from 0.25 mm to about 1.27 mm. This spacing permits at least three traces 22 to pass between side-by-side capture pads 20.

In Fig. 6, circuit 10 includes a substrate including a first dielectric layer 12a and a second dielectric layer 13. First dielectric layer 12a includes a first surface 14a and a second surface 16a. A conductive layer 18a is provided on first surface 14a between first dielectric layer 12a and second dielectric layer 13. A beveled via 24 is formed in first dielectric layer 12a as described and referred to above. Also, the second dielectric layer 13 may be formed of a polymer material as described above. One of the layers 12a and 13 may be provided as a cover coat for the other layer.

Well known tape ball grid array (TBGA) package typically includes a substrate having an integrated circuit (IC) mounted in a cavity that is surrounded by an array of vias. Leads from the IC interconnect to the vias. One embodiment herein, Figs. 7 and 8, discloses a substantial improvement such that the substrate is substantially of the same surface area as the IC. This is possible due to the reduced size openings of the tapered vias as described above. Thus, the advantages provided by the reduced size openings permits increased trace routing between the vias. Also, the opposite or larger via openings provide increased surface contact to improve solder ball shear strength. The chip scale package 100, Fig. 7, includes a substrate 112 having a first surface 114 and a second surface 116. A surface area A1 of first surface 114 is substantially the same as a second surface area A2 of an IC 150 mounted on substrate 112. A conductive layer 118 on portions of first surface 114 area is connected to IC 150 by leads 152. An adhesive layer 155 on surface 114 of

substrate 112, and an adhesive layer 157 on IC 150 are interconnected by an interposer layer 154 therebetween. The interposer layer 154 may, for example, be a compliant material such as a foam or elastomeric material, or a non-compliant material such as a ceramic or a copper sheet. Substrate 112 includes a plurality of beveled vias 124, as described above. Each via includes a first opening 126 in first surface 114 and a second opening 128 in second surface 116. The second width being greater than the first width as herein described. A plug 132 is provided in each via to extend from adjacent the first opening 126 to adjacent the second opening 128 and terminating at a plug interface surface 136. A conductive solder ball 138 is connected to the plug interface surface 136 and extends to protrude from second surface 116 for connection to a printed circuit board 144. Thus, a plurality of solder balls 138 provide an array which is uniform across second surface 116 of substrate 112, without interruption by a commonly heretofore known space required for mounting an IC package on opposite surface 114.

As it can be seen, the principal advantages of these embodiments are that the via plug adapter enables a reliable solder ball connection to flexible circuitry with small (less than 0.200 mm diameter) vias. Using the via plug adapter concept, solder ball interconnection reliability does not have to be compromised to accommodate the routing requirements of high I/O, fine pitch flex based IC packaging applications. Using common design rules for flexible circuitry, a smaller via allows for a smaller via capture pad, thus, more space between via capture pads in which to route electronic traces. As an example, using a via plug adapter in a 0.085 mm diameter beveled via, 4 traces can be routed between capture pads with similar solder ball interconnection reliability as with 0.300 mm diameter vias that only allow routing of a single trace.

The foregoing describes a flexible circuit with a z-axis via interconnection between fine feature flexible circuitry and gross feature printed circuit board solder ball pads using traditional solder balls with the novel use of a via plug adapter. One such application of this via plug adapter is the flexible circuit application in IC packaging for BGA to printed circuit board interconnection.

The via plug adapter is a metal plug additively plated into a beveled via. In addition to forming the plug using an additive plating process, a process such as solder reflow could be used to form the via plug. This via plug adapter is a frustum

(the solid of a cone between two parallel planes) shaped metal feature with a slight dome shape at the second interface surface. As the z-direction thickness of the frustum grows within the beveled via, the surface area for traditional solder ball attachment grows dramatically creating a mechanical adapter allowing small vias to
5 have similar solder ball interconnection reliability as with large via applications.

Allowing small vias in the flexible circuit improves the routability of the flexible circuit to address higher I/O and finer pitch flex based BGA packaging applications.

As a result, one embodiment provides a circuit comprising a substrate
10 including a dielectric layer having a first surface and a second surface. A conductive layer is on the first surface. A beveled via is formed in the dielectric layer. The via has a first opening of a first width in the first surface and a second opening of a second width, in the second surface, greater than the first width. A conductive plug is connected to the conductive layer and is formed in the via and extends from adjacent
15 the first opening toward the second opening. The plug terminates adjacent the second opening at a plug interface surface. A conductive solder ball is connected to the plug interface surface, and extends to protrude from the second surface.

Another embodiment provides a circuit comprising a substrate including a dielectric layer having a first surface and a second surface. A conducted layer is on
20 the first surface. A beveled via is formed in the dielectric layer. The via has a first opening of a first width in the first surface and a second opening of a second width in the second surface, greater than the first width. A conductive plug is connected to the conductive layer and is formed in the via and extends from adjacent the first opening toward the second opening. The plug terminates adjacent the second opening at a
25 plug interface surface. A conductive solder ball has a first solder ball surface connected to the plug interface surface. The solder ball extends to protrude from the second surface and terminates at a second solder ball surface. A printed circuit board is engaged with the second solder ball surface.

In still another embodiment, a circuit comprises a substrate including a
30 dielectric layer having a first surface and a second surface. A pair of side-by-side beveled vias are formed in the dielectric layer. Each via has a first opening of a first width in the first surface, and a second opening of a second width in the second surface, greater than the first width. Each via includes a conductive plug having a

first plug interface surface adjacent the first opening. Each plug extends from adjacent the first plug interface surface toward the second opening. Each plug terminates adjacent the second opening at a second plug interface surface. A conductive solder ball is formed at each via and has a first solder ball surface engaged with its respective second plug interface surface, and extends to protrude from the second surface. Each solder ball terminates at a second solder ball surface. A printed circuit board is engaged with the second solder ball surface. A conductive capture pad layer is engaged with the first interface surface of each plug to form side-by-side, spaced apart, capture pad layers. A plurality of conductive traces extend between the side-by-side capture pad layers.

A further embodiment provides a method of attaching a solder ball to a via in a flexible circuit substrate. This is accomplished by forming a beveled via in the flexible circuit substrate having a first surface and a second surface. A first via opening is formed in the first surface and has a first width. A second via opening is formed in the second surface and has a second width, greater than the first width. A conductive layer is formed at the first opening. A conductive plug is formed in the beveled via connected to the conductive layer so that the plug extends from adjacent the first surface toward the second surface. The plug terminates at a plug interface surface adjacent the second surface. A conductive solder ball is engaged with the plug interface surface. The solder ball extends to protrude from the second surface.

Although illustrative embodiments have been shown and described, a wide range of modifications, change and substitution is contemplated in the foregoing disclosure and in some instances, some features of the embodiments may be employed without a corresponding use of other features. Accordingly, it is appropriate that the appended claims be construed broadly and in a manner consistent with the scope of the embodiments disclosed herein.

What is claimed is:

1. A circuit comprising:
a substrate including a dielectric layer having a first surface and a second surface;
5 a conductive layer on the first surface,
wherein the dielectric layer and conductive layer form a flexible circuit;
a beveled via formed in the dielectric layer, the via having a first opening of a first width in the first surface, and a second opening of a second width in the second surface, the second width being greater than the first width;
10 a conductive plug connected to the conductive layer, the plug being formed in the via, and extending from adjacent the first opening toward the second opening, and terminating adjacent the second opening at a plug interface surface; and
a conductive solder ball connected to the plug interface surface and extending to protrude from the second surface.
- 15 2. The circuit as defined in claim 1, wherein the dielectric layer is formed of a polymer material selected from polyimide and polyester, such material having a thickness of from 12 micrometers to 125 micrometers.
3. The circuit as defined in claim 1 wherein the beveled via has a sidewall sloped away from the first surface at an angle of from 20 degrees to 80 degrees.
- 20 4. The circuit as defined in claim 1 wherein the plug interface surface forms a dome.
5. The circuit as defined in claim 4 wherein the dome is between the first surface and the second surface.
6. The circuit as defined in claim 4 wherein a portion of the dome extends
25 outwardly from the second surface.
7. The circuit as defined in claim 1 wherein the plug has a thickness dimension extending from the first surface to the dome, the thickness dimension being at least 5 microns.

8. The circuit as defined in claim 1 wherein the ball is formed of a tin-lead solder and the plug is formed of a conductive material and has a stronger shear strength than the tin-lead solder.

9. The circuit as defined in claim 1 wherein the conductive layer is
5 formed of copper or gold.

10. The circuit as defined in claim 9 further comprising:
an interface coating between the conductive layer and the plug, the coating
being selected from the group consisting of gold, paladium and nickel-gold.

11. The circuit as defined in claim 9 further comprising:
10 an interface coating between the interface surface of the plug and the ball, the
coating being selected from the group consisting of gold, paladium and nickel-gold.

12. A circuit comprising:
a substrate including a dielectric layer having a first surface and a second
surface;
15 a pair of side-by-side beveled vias formed in the dielectric layer, each via
having a first opening of a first width in the first surface and a second opening of a
second width in the second surface, the second width being greater than the first
width;

each via including a conductive plug having a first plug interface surface
20 adjacent the first opening, each plug extending from adjacent the first plug interface
toward the second opening, each plug terminating adjacent the second opening at a
second plug interface surface;

a conductive solder ball formed at each via, each solder ball having a first
solder ball surface engaged with its respective second plug interface surface, and
25 extending to protrude from the second surface, each solder ball terminating at a
second solder ball surface;

a printed circuit board engaged with the second solder ball surface;

a conductive capture pad layer engaged with the first interface surface of each
plug to form side-by-side, spaced apart capture pad layers; and

a plurality of conductive traces extending between the side-by-side capture pad layers.

13. The circuit as defined in claim 12 wherein the plurality of conductive traces includes at least three traces.

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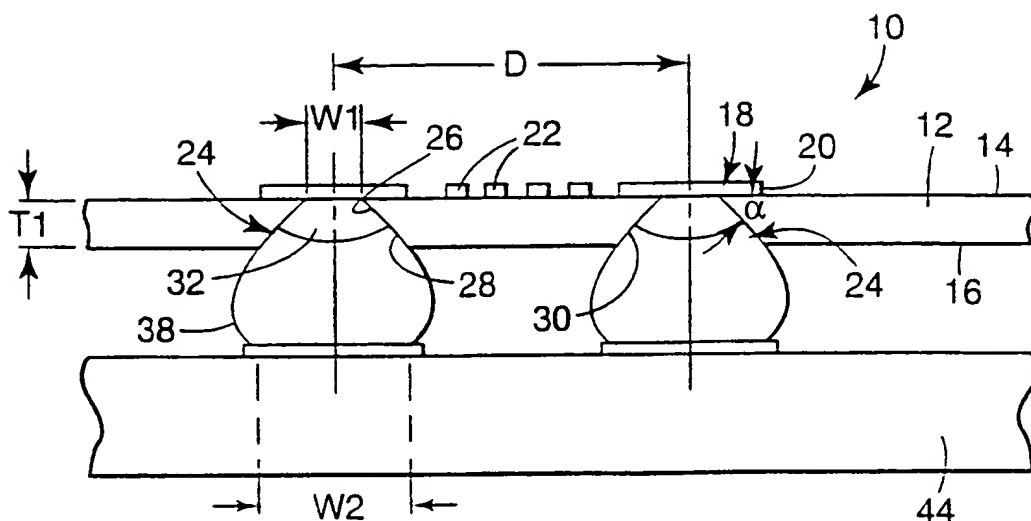


Fig. 1

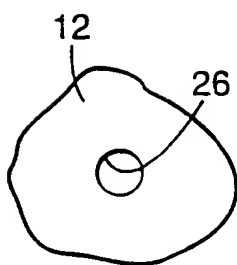


Fig. 1A

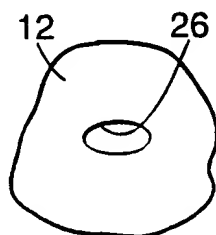


Fig. 1B

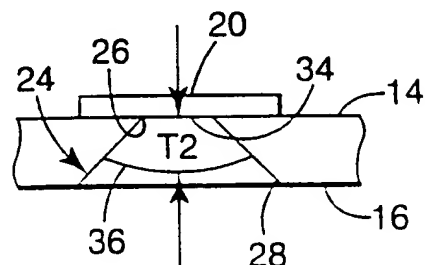


Fig. 2

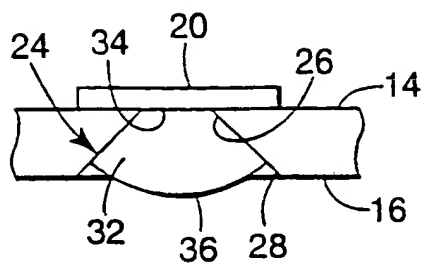


Fig. 3

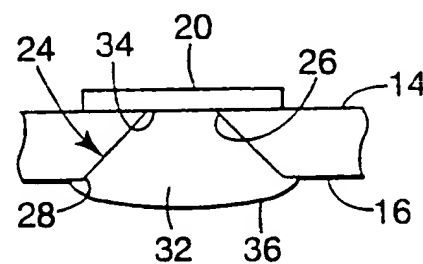
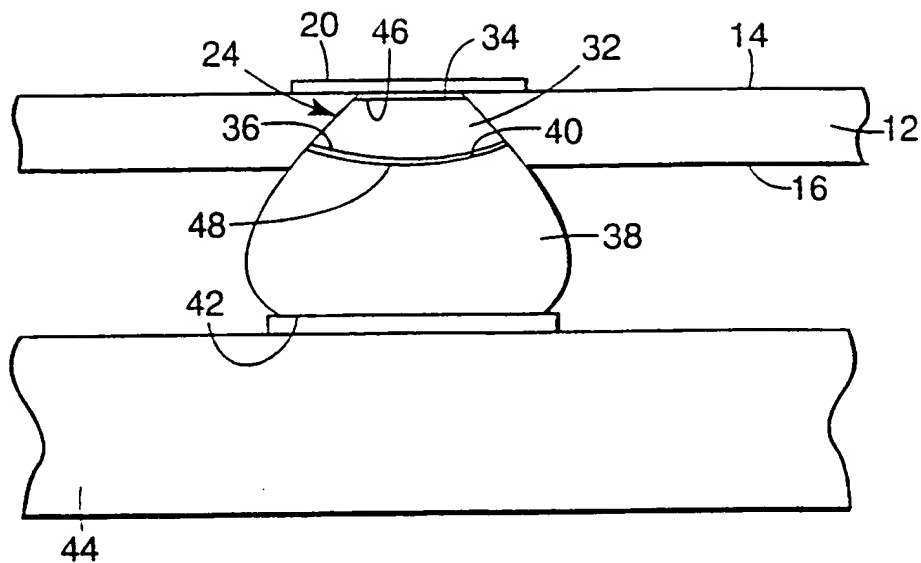
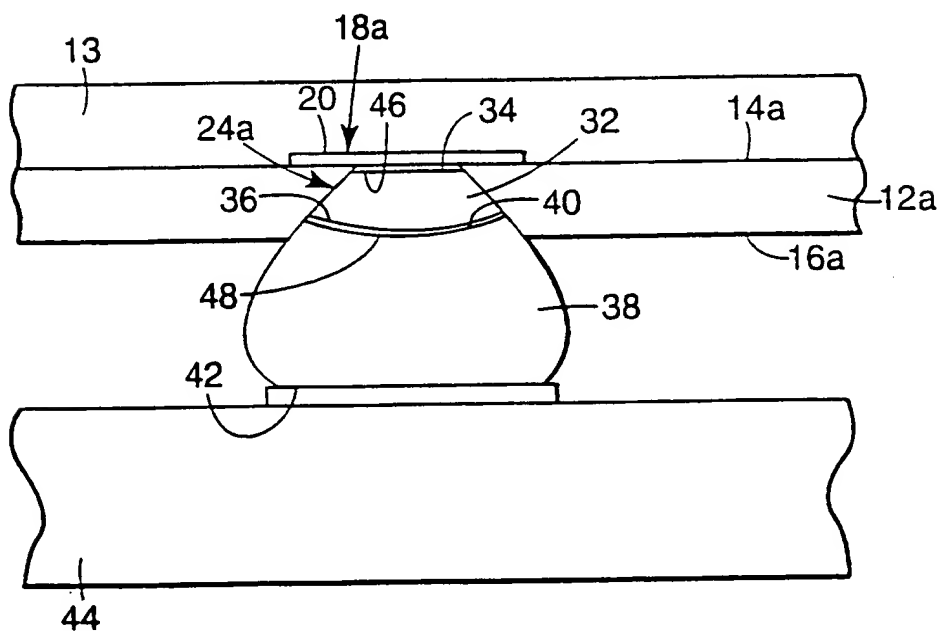


Fig. 4

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**Fig. 5****Fig. 6**

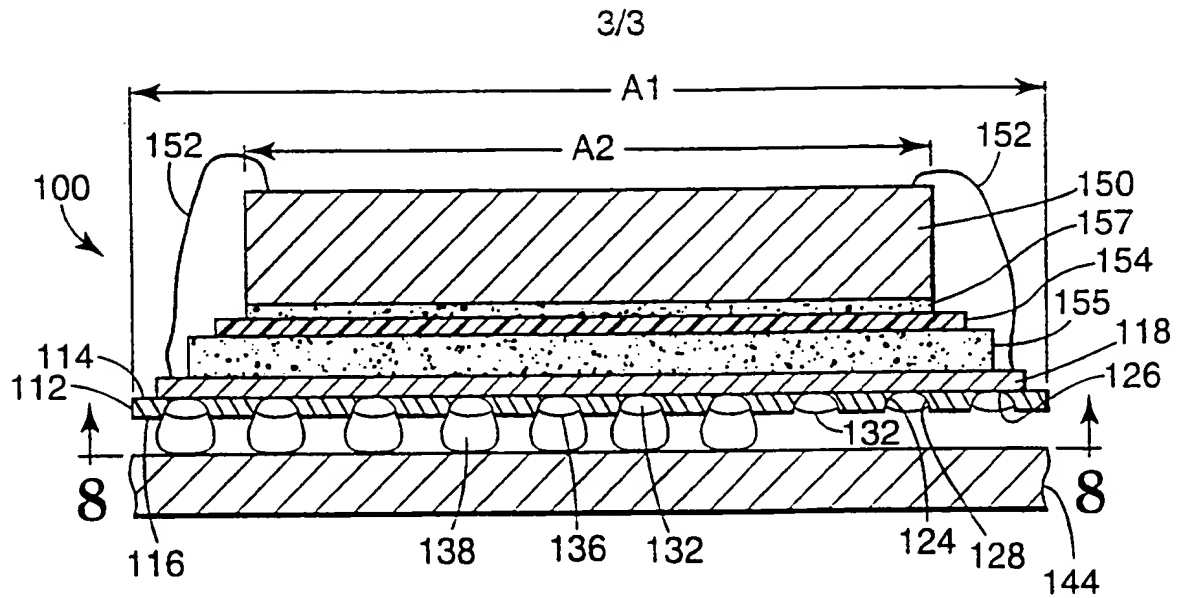


Fig. 7

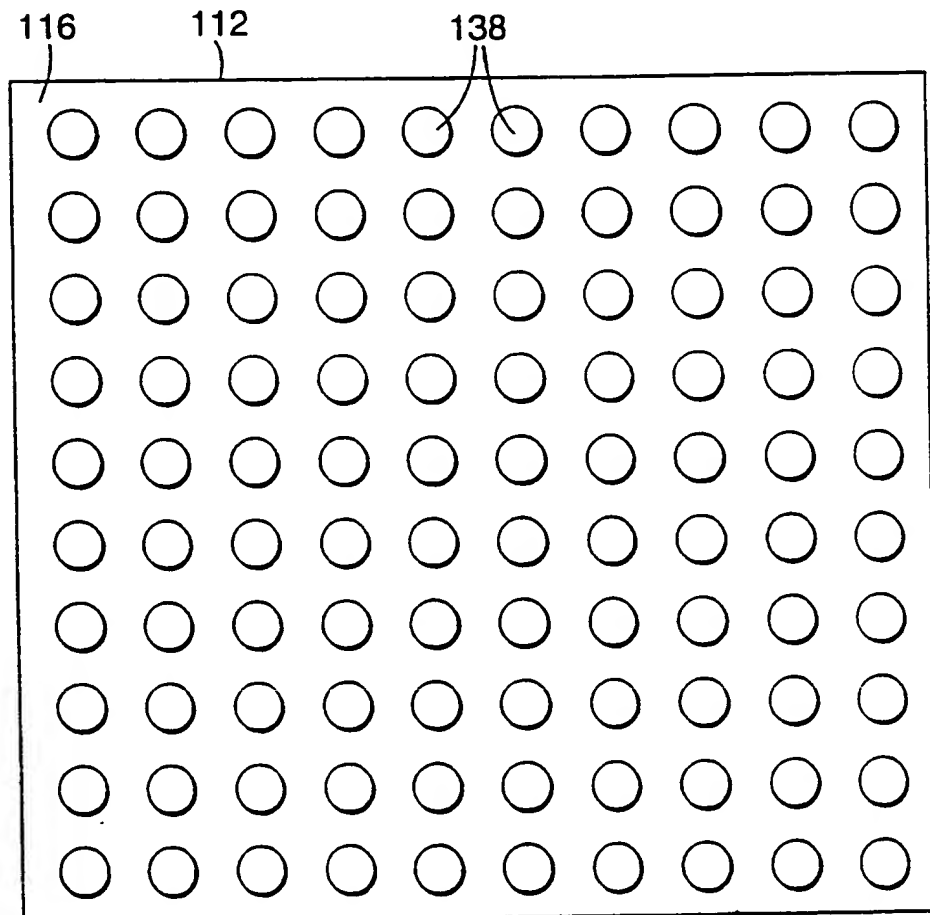


Fig. 8

INTERNATIONAL SEARCH REPORT

National Application No.

EP/US 99/00179

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L23/498

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	DE 197 02 014 A (FRAUNHOFER GES FORSCHUNG) 16 April 1998 see the whole document ---	1-4, 6-9, 12, 13
Y	EP 0 751 565 A (NITTO DENKO CORP) 2 January 1997 see the whole document ---	1-4, 6-9, 12, 13
A	EP 0 702 404 A (NIPPON ELECTRIC CO) 20 March 1996 see figures 3A, 3B ---	1-13
A	US 5 203 075 A (ANGULAS CHRISTOPHER G ET AL) 20 April 1993 see figure 6 ---	1, 12
A	US 5 663 594 A (KIMURA NAOTO) 2 September 1997 -----	

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Further documents are listed in the continuation of box C.

☒

Patent family members are listed in annex.

* Special categories of cited documents :

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- "&" document member of the same patent family

Date of the actual completion of the international search

20 April 1999

Date of mailing of the international search report

27/04/1999

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Prohaska, G

INTERNATIONAL SEARCH REPORT

International Application No.

Information on patent family members

PCT/US 99/00179

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